PI3DSB12212A application information

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1. Introduction

Thunderbolt, SAS 3.0, USB3.1, PCIe G3 and many protocol new revisions request a switch with bandwidth up to 12Gbpd, such as PI3DBS12212A.

2. Typical Application Circuit

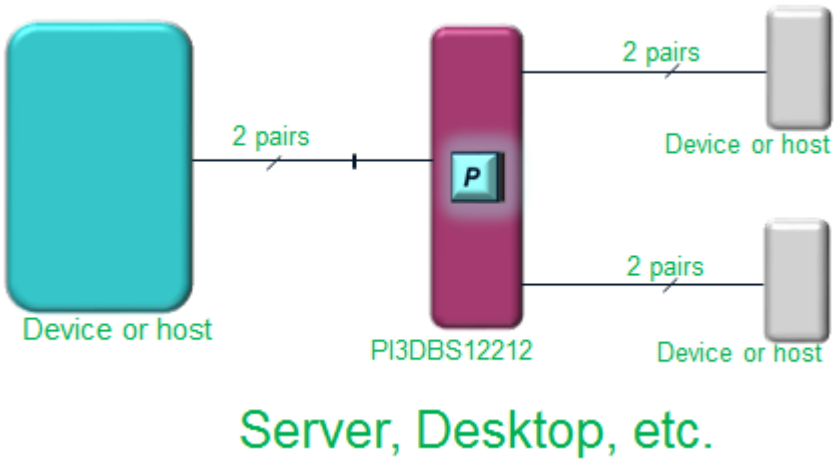

Figure 1: PI3DBS12212A application topologie

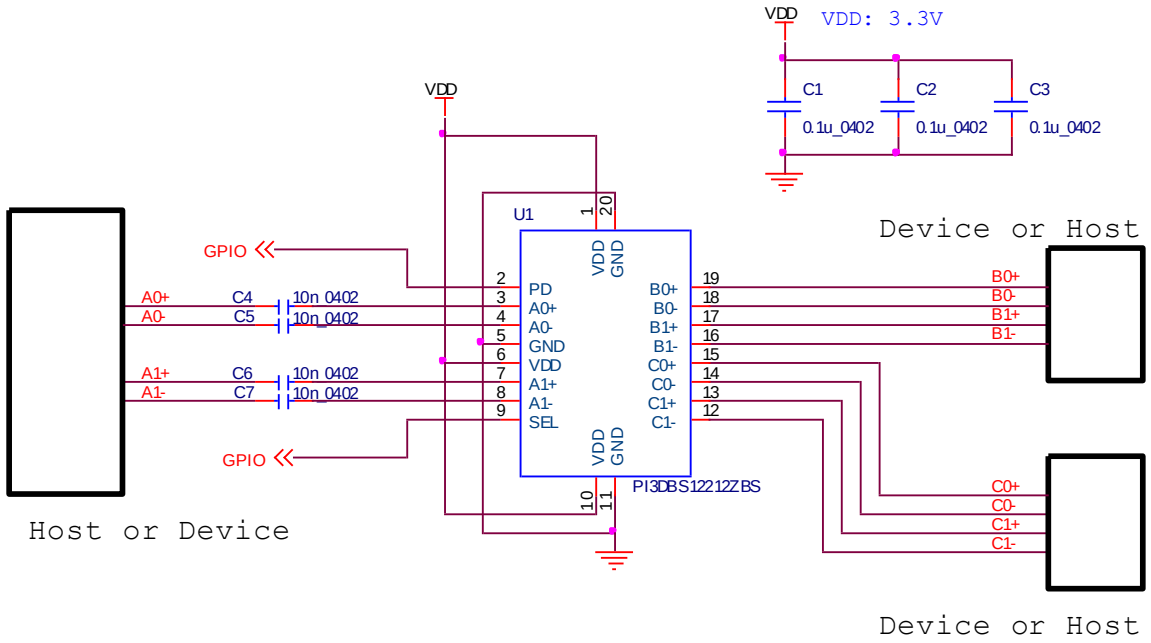

Figure 2, PI3DBS12212AZBS@TQFN20 application schematic

3. Main Link Channels

In applications (figure 1, 2, 3), AC coupling capacitors can be either between host-PI3DBS12212A or between device-PI3DBS12212A.
Assure the signals going thru PI3DBS12212A is in the range of -0.5V to 1.6V single-ended, which is the allowable working voltage range of PI3DBS12212A.

4. Control Pins

OE1# and OE2# pins can be tied to ground. Use a system GPIO to control SEL pin.

5. Differential insertion loss

Figure-4 is the differential insertion loss of PI3DBS12212A.

Figure-4, the -1.2493db /5.646Ghz (11.2Gbps) differential insertion loss of PI3BDS12412A (reference for PI3DBS12212A)

6 Layout and power

90ohm differential impedance

Plane	Material	Thickness (mil)
Solder mask	Mask paint	1.2
Signal	Copper	1.9
Prepreg	2116	4.4
Vcc	Copper	1.4
Core		47
Vss	Copper	1.4
Prepreg	2116	4.4
Signal	Copper	1.9
Solder mask	Mask paint	1.2
Total		62.4

Table-2, the stack-up of 90ohm differential impedance

- Use 6-7-6 mils for trace-space-trace for the micro-strip lines (the traces on top and bottom layers) for 90ohm differential impedance.
- Use 6-5-6 mils for trace-space-trace for the strip-lines (the traces inside layers) for 90ohm differential impedance.

- Use FR4.
- Using standard 4 to 8 layers stack-up with 0.062 inch thick PCB.
- For micro-strip lines, using ½ OZ Cu plated is ok.
- For strip-lines in 6 plus players, using 1 OZ Cu is better.
- More pair-to-pair spacing for minimal crosstalk
- Target differential Zo of 90ohm ±15ohm
- The above is only for generic reference. Impedance shall be controlled in PCB fabrication.

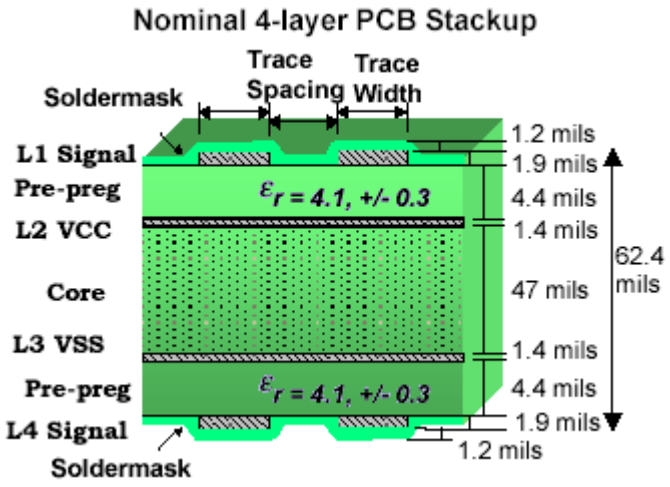

Figure 13, the PCB layers stack-up

The layout of traces

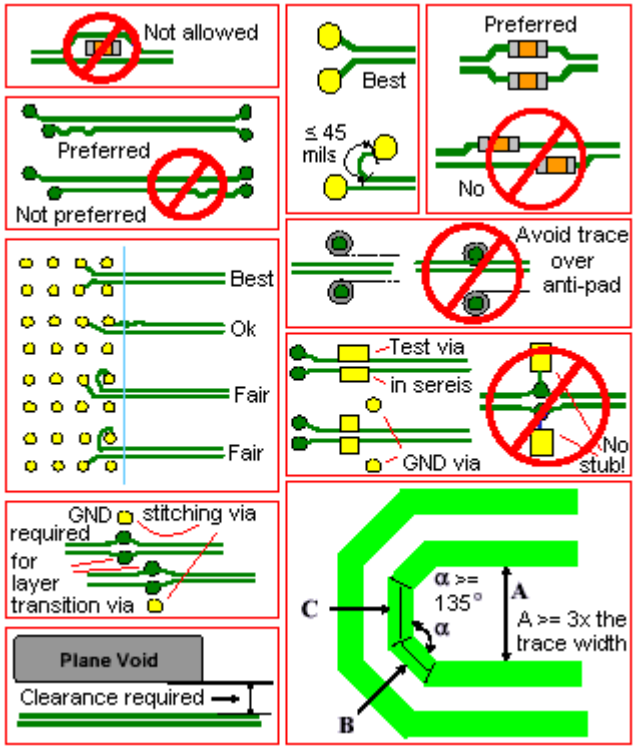

Figure 14, the layout of traces

VDD bypass capacitance and power-ground layers

- Use 0.1uf in size of 0402 for all the VDD (any power pins) pins of the IC device, as close to the VDD pins as possible, within 2-3mm if feasible.
- Use dedicated VDD and GND planes if feasible to minimize the power noise.